

N-Ch 100V Fast Switching MOSFETs

Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

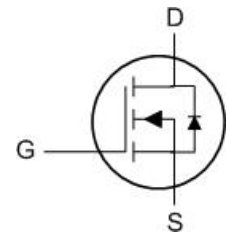
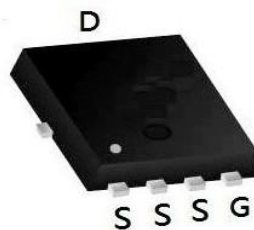
- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

Product Summary



BVDSS	RDSON	ID
100V	61mΩ	15A

PDFN3333-8L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	15	A
$I_D @ T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	10.7	A
I_{DM}	Pulsed Drain Current ²	80	A
EAS	Single Pulse Avalanche Energy ³	22	mJ
I_{AS}	Avalanche Current	---	A
$P_D @ T_C=25^\circ\text{C}$	Total Power Dissipation ⁴	46	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	---	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	2.7	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	100	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA	---	---	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =5A	---	61	75	mΩ
		V _{GS} =4.5V, I _D =4A	---	77	100	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.3	1.8	2.3	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	---	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =100V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =100V, V _{GS} =0V, T _J =100°C	---	---	100	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =5A	---	---	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	---	---	Ω
Q _g	Total Gate Charge	V _{DS} =50V, V _{GS} =10V, I _D =10A	---	3.7	---	nC
Q _{gs}	Gate-Source Charge		---	0.8	---	
Q _{gd}	Gate-Drain Charge		---	1	---	
T _{d(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DD} =50V, R _G =3Ω, I _D =10A	---	8	---	ns
T _r	Rise Time		---	16	---	
T _{d(off)}	Turn-Off Delay Time		---	17	---	
T _f	Fall Time		---	14	---	
C _{iss}	Input Capacitance	V _{DS} =50V, V _{GS} =0V, f=1MHz	---	228	---	pF
C _{oss}	Output Capacitance		---	58	---	
C _{rss}	Reverse Transfer Capacitance		---	1.9	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	15	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =20A, T _J =25°C	---	---	1.2	V
t _{rr}	Reverse Recovery Time	I _F =10A, di/dt=100A/μs, T _J =25°C	---	22	---	nS
Q _{rr}	Reverse Recovery Charge		---	18	---	nC

Note :

F The data is tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.

G The data is tested by pulsed pulse width ≤ 300us duty cycle ≤ 2%

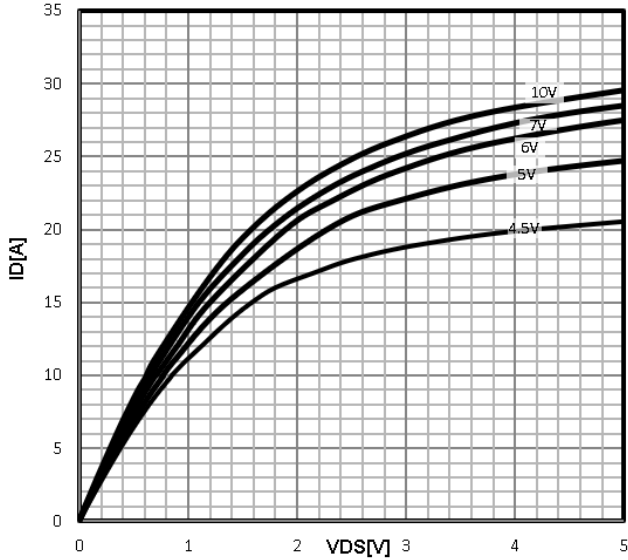
H The EAS data shows Max. rating. The test condition is V_{RMS} = 0, V_{DD}=50V, V_{GS}=10V, L=5mH.

I The power dissipation is limited by 150°C junction temperature

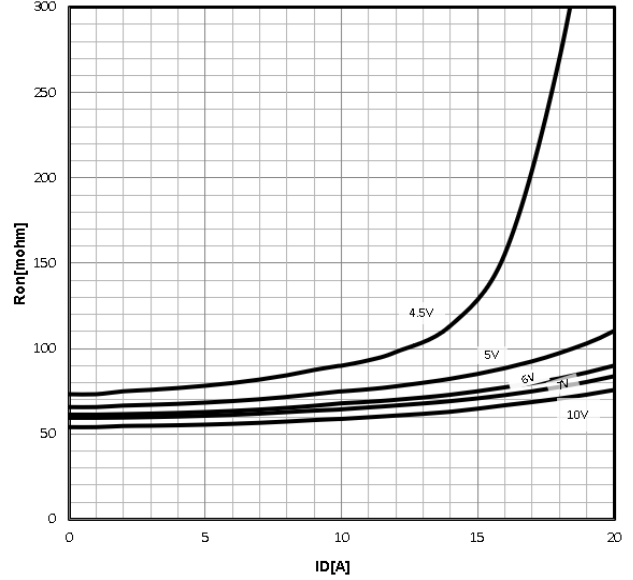
J The data is theoretically the same as A_{DM} and A_{DM} in real applications should be limited by total power dissipation.

Characteristics Curve:

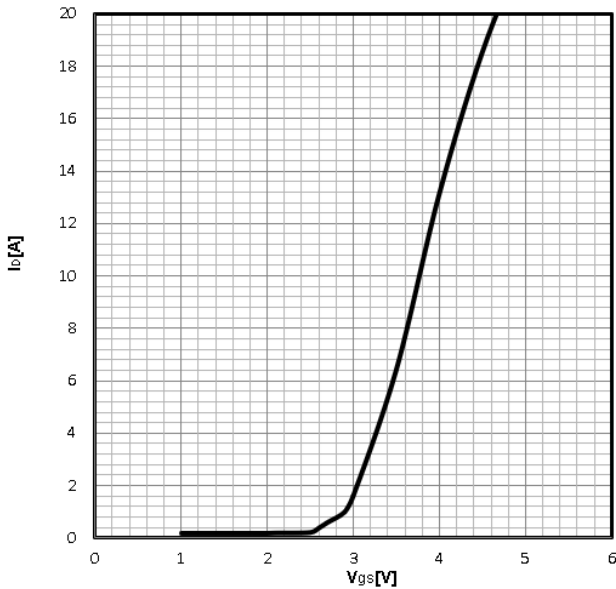
Typ. output characteristics
 $I_D = f(V_{DS})$



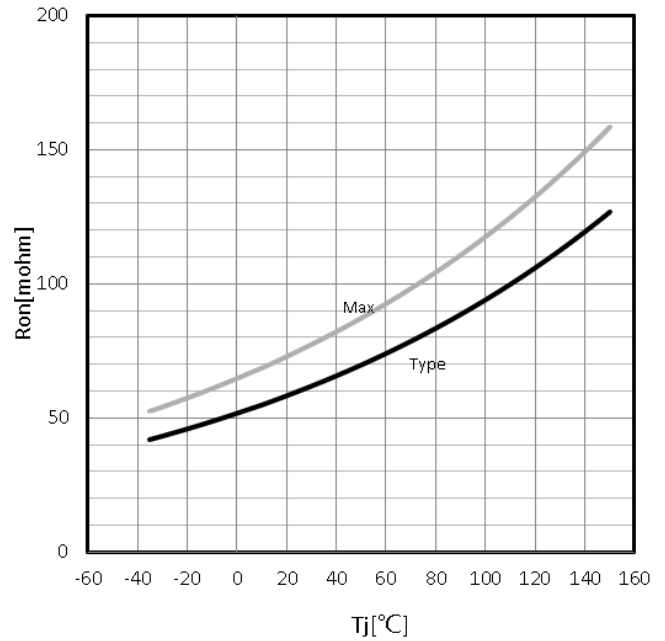
Typ. drain-source on resistance
 $R_{DS(on)} = f(I_D)$



Typ. transfer characteristics
 $I_D = f(V_{GS})$

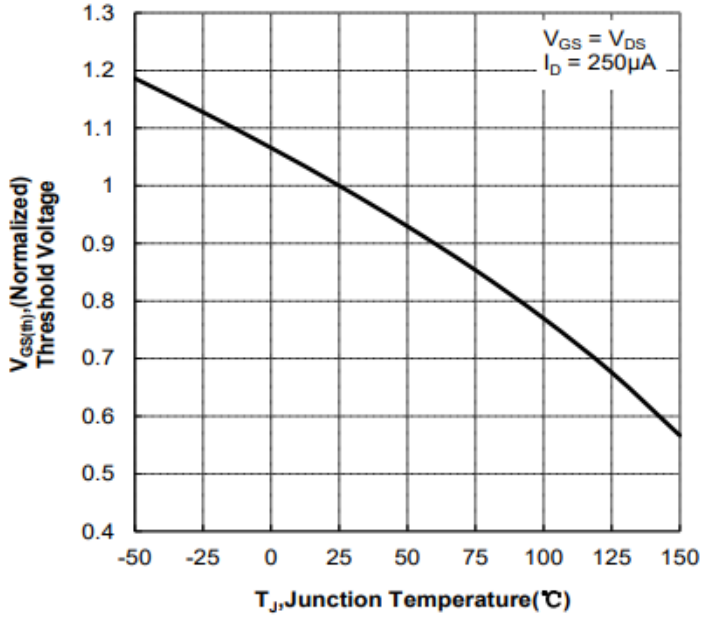


Drain-source on-state resistance
 $R_{DS(on)} = f(T_j); I_D = 5A; V_{GS} = 10V$



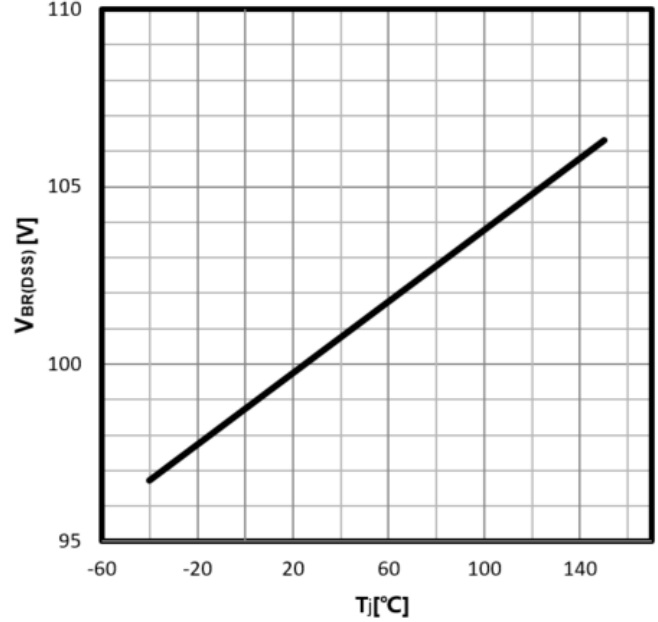
Gate Threshold Voltage

$V_{TH}=f(T_j); I_D=250\mu A$



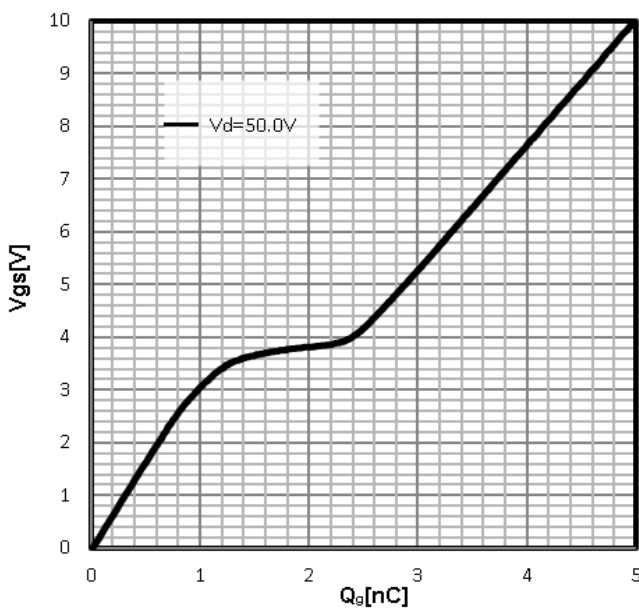
Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=250\mu A$



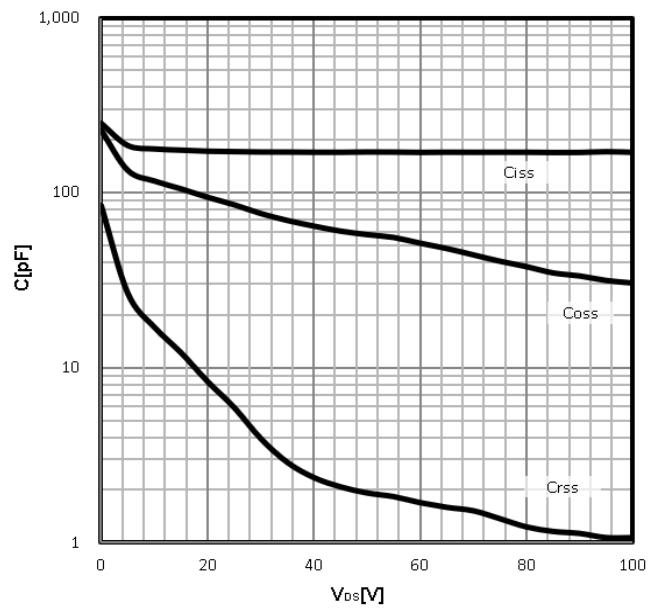
Typ. gate charge

$V_{GS}=f(Q_g); I_D=10A$

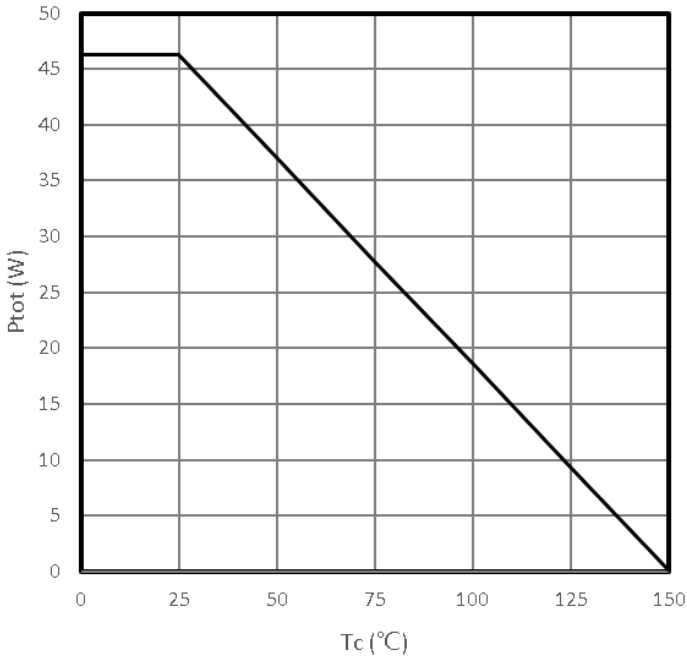


Typ. capacitances

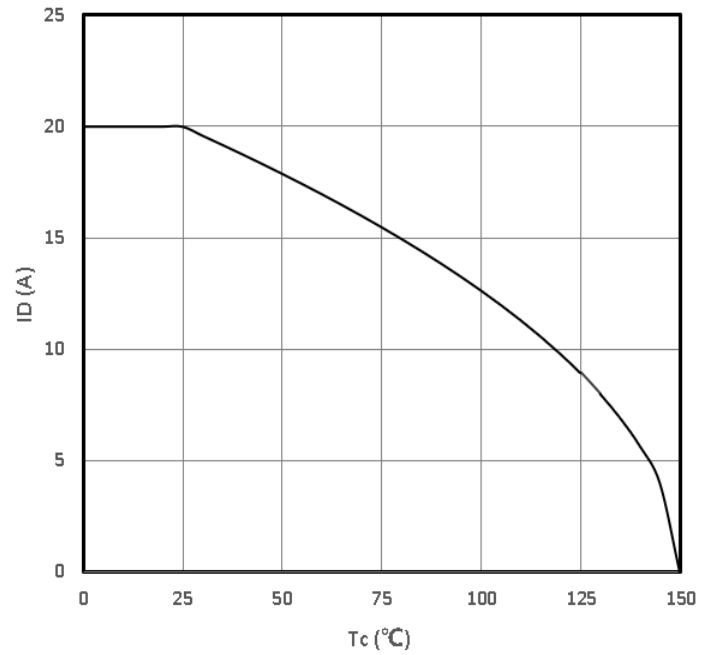
$C=f(V_{DS}); V_{GS}=0V; f=1MHz$



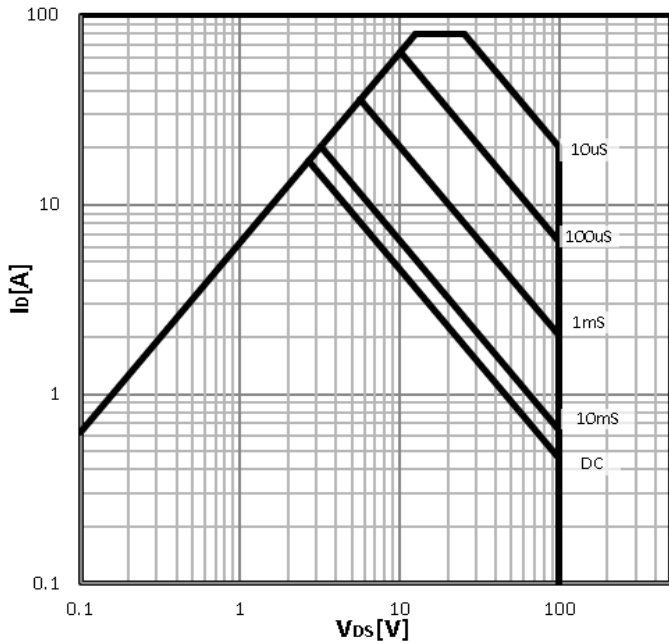
Power Dissipation
 $P_{tot}=f(T_c)$



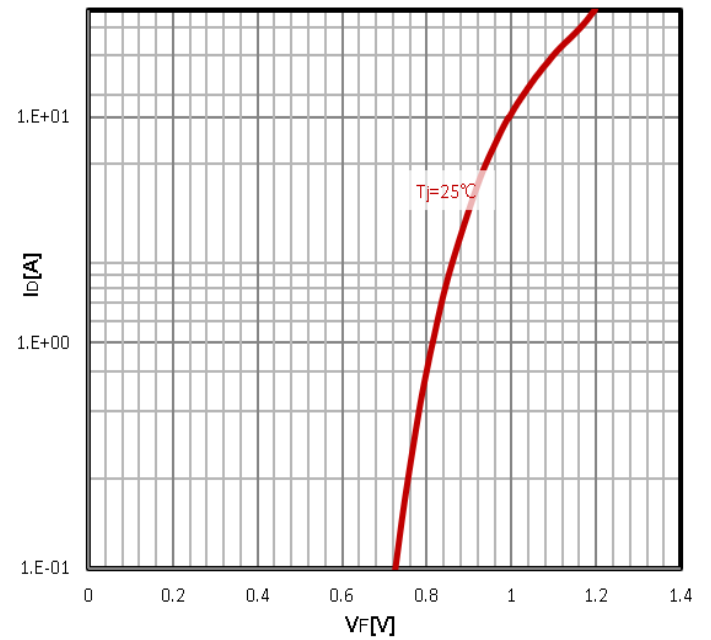
Maximum Drain Current
 $I_D=f(T_c)$



Safe operating area
 $I_D=f(V_{DS})$

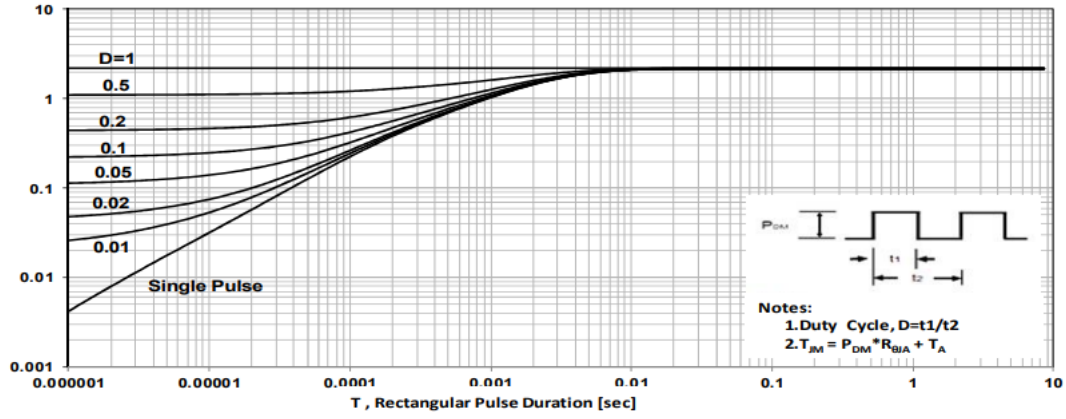


Body Diode Forward Voltage Variation
 $I_F=f(V_{GS})$

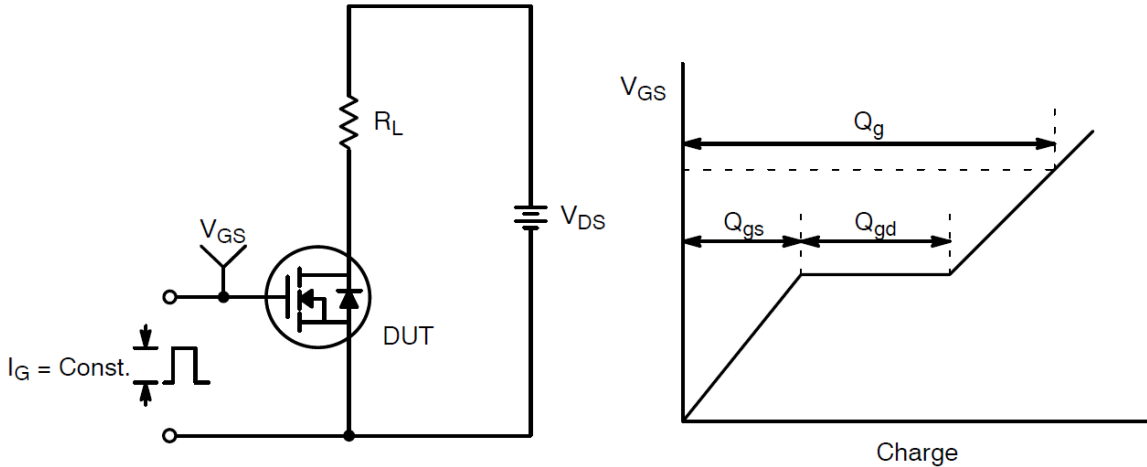


Max. transient thermal impedance

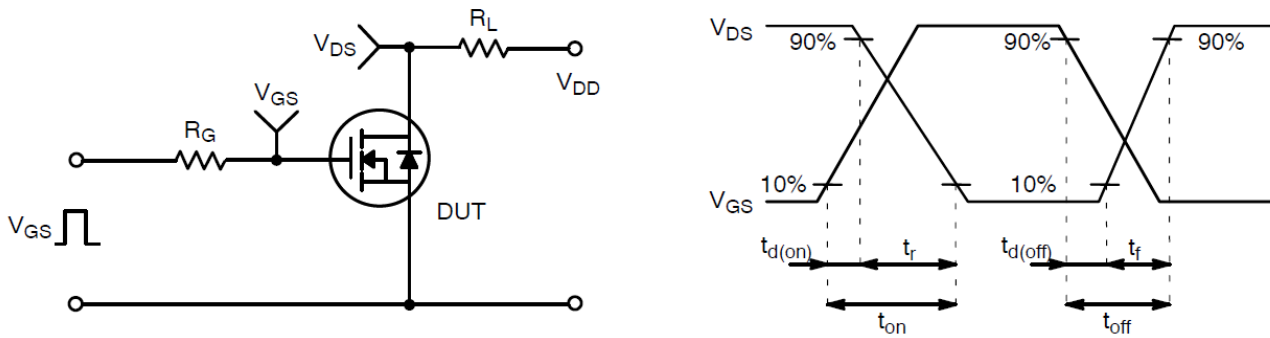
$$Z_{thJC}=f(t_p)$$



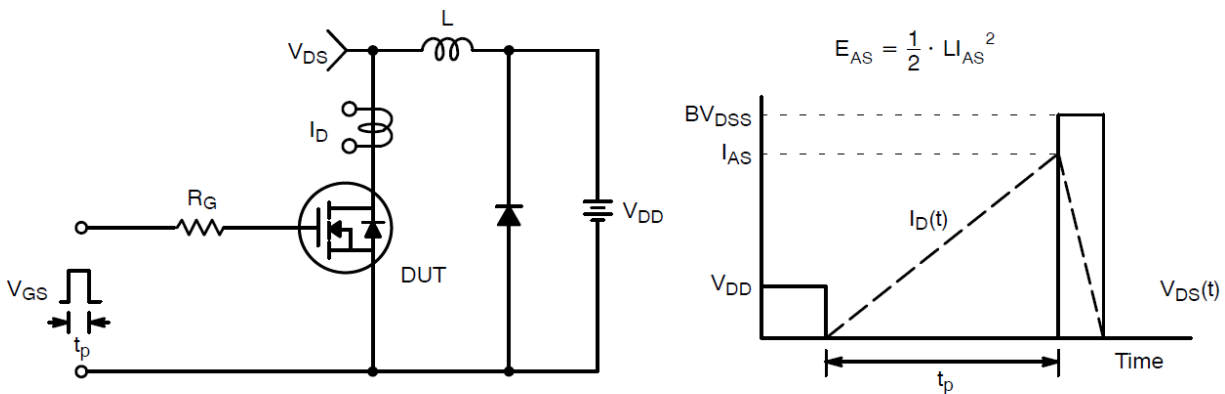
Test Circuit and Waveform:



Gate Charge Test Circuit & Waveform

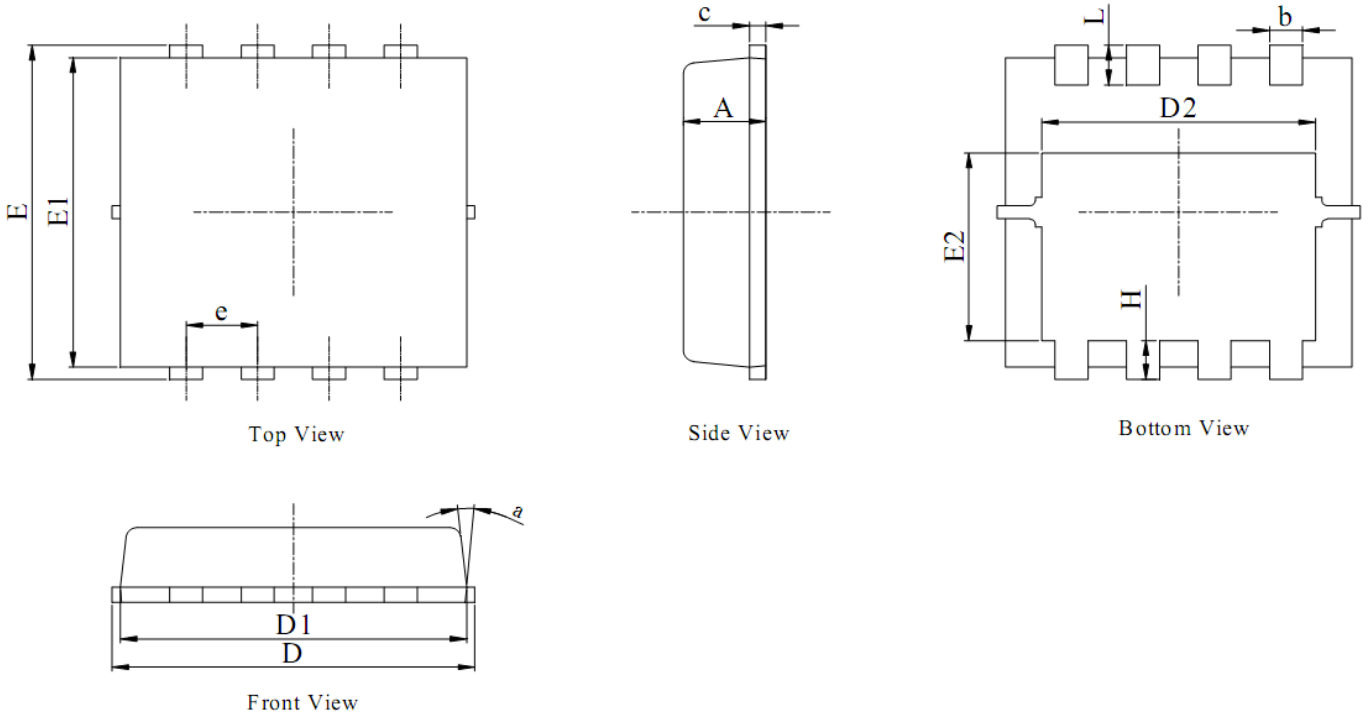


Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

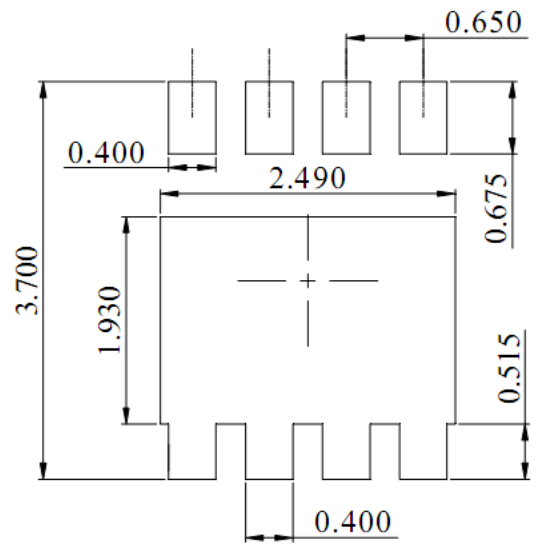
Package Mechanical Data-PDFN3333-8L-Single



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMENSIONS IN MILLIMETER (ANGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.20	0.25
D	3.00	3.15	3.25
D1	2.95	3.05	3.15
D2	2.39	2.49	2.59
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.70	1.80	1.90
e	0.65 BSC		
H	0.30	0.40	0.50
L	0.25	0.40	0.50
a	---	---	15°



DIMENSIONS: MILLIMETERS