P-Ch 40V Fast Switching MOSFETs

★ 100% EAS Guaranteed
★ Green Device Available
★ Super Low Gate Charge
★ Excellent CdV/dt effect decline
★ Advanced high cell density Trench technology

Product Summary

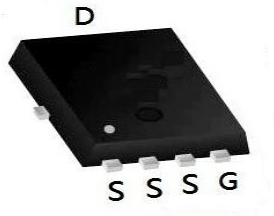
Green

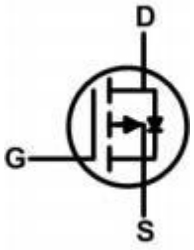
BVDSS	RDSON	ID
-40V	3.1mΩ	-100A

Description

The XR100P04F is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.
The XR100P04F meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

PDFN5060-8L Pin Configuration





Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-40	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1,6]	-100	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1,6]	-70	A
I_{DM}	Pulsed Drain Current[2]	-400	A
EAS	Single Pulse Avalanche Energy[3]	1225	mJ
I_{AS}	Avalanche Current	---	A
P_D@T_C=25℃	Total Power Dissipation[4]	200	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	---	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	0.95	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-40	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	---	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-13A	---	3.1	4.1	mΩ
		V_{GS}=-4.5V , I_D=-13A	---	4.4	5.4	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.2	---	-2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	---	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-40V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-40V , V_{GS}=0V , T_J=55℃	---	---	-100	
I_{GSS}	Gate-Source Leakage Current	V_{GS}= ±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-10V , I_D=-13A	---	51	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	1.7	---	Ω
Q_g	Total Gate Charge	V_{DS}=-20V , V_{GS}=-10V , I_D=-13A	---	195	---	nC
Q_{gs}	Gate-Source Charge		---	24.1	---	
Q_{gd}	Gate-Drain Charge		---	39.9	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-20V , V_{GS}=-10V , R_G=3.3Ω	---	19.6	---	ns
T_r	Rise Time		---	3.6	---	
$T_{d(off)}$	Turn-Off Delay Time		---	22.8	---	
T_f	Fall Time		---	38	---	
C_{iss}	Input Capacitance	V_{DS}=-20V , V_{GS}=0V , f=1MHz	---	10733	---	pF
C_{oss}	Output Capacitance		---	770	---	
C_{rss}	Reverse Transfer Capacitance		---	697	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	-100	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-13A , T_J=25℃	---	---	-1.2	V
t_{rr}	Reverse Recovery Time	IF=-13A , di/dt=100A/μs , T_J=25℃	---	51.1	---	nS
Q_{rr}	Reverse Recovery Charge		---	125.2	---	nC

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is TJ=25℃,VDD=-40V,VG=-10V, Rg=25Ω, L=0.5mH.
4.The power dissipation is limited by 150℃ junction temperature
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Electrical And Thermal Characteristics (Curves)

Figure 1. Output Characteristics

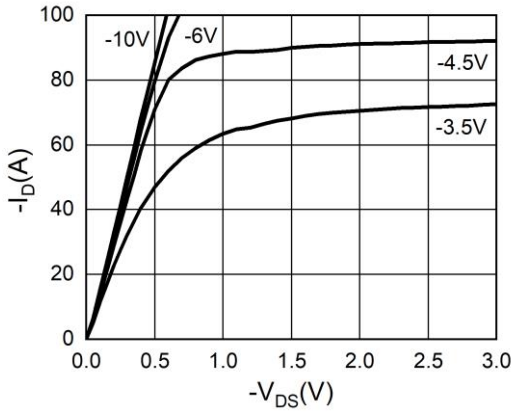


Figure 2. Transfer Characteristics

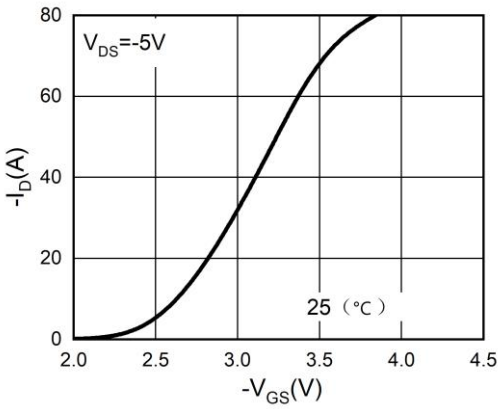


Figure 3. Power Dissipation

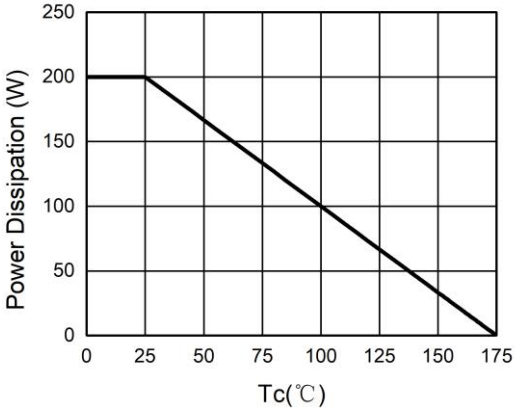


Figure 4. Drain Current

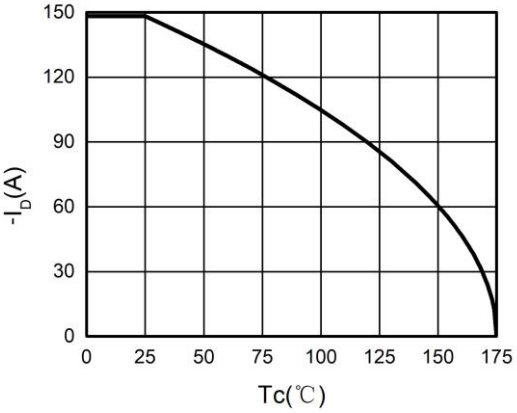


Figure 5. BV_{DSS} vs Junction Temperature

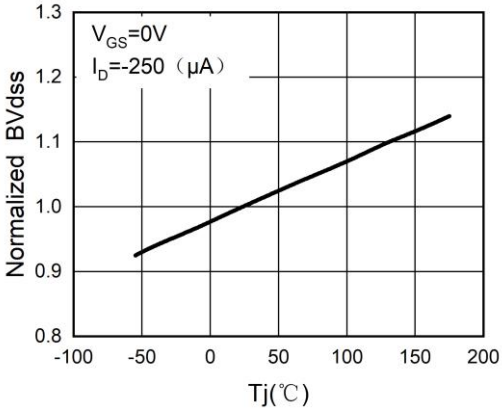
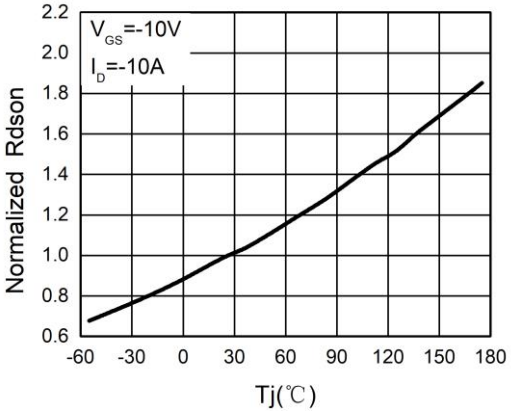


Figure 6. $R_{DS(ON)}$ vs Junction Temperature



Typical Electrical And Thermal Characteristics (Curves)

Figure 7. Gate Charge Waveforms

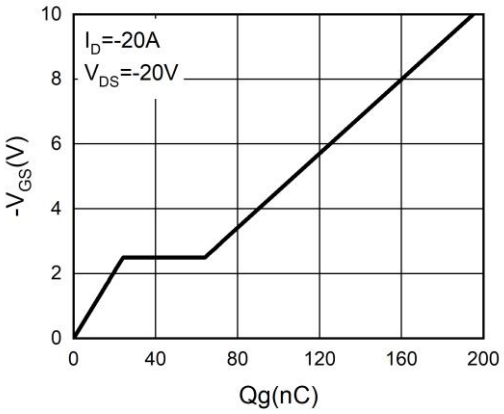


Figure 8. Capacitance

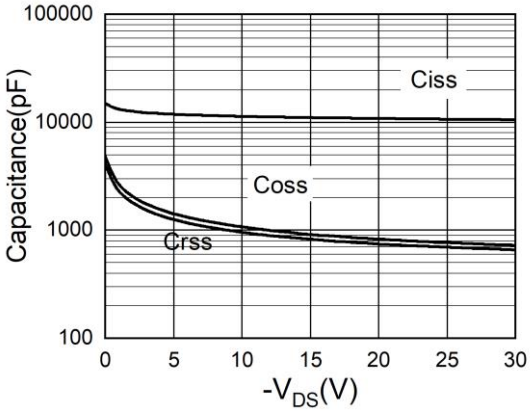


Figure 9. Body-Diode Characteristics

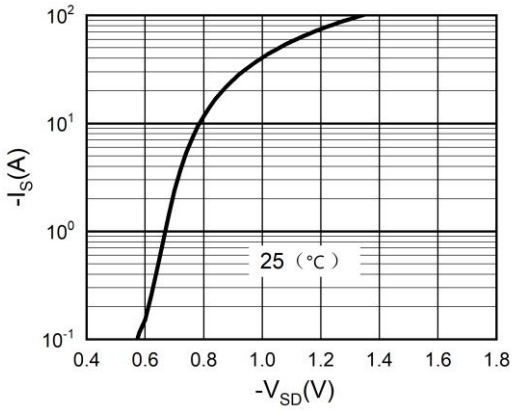
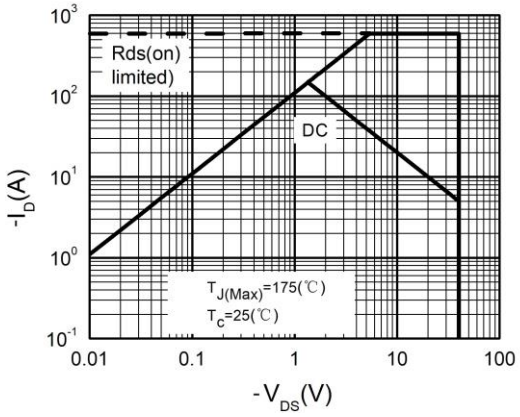
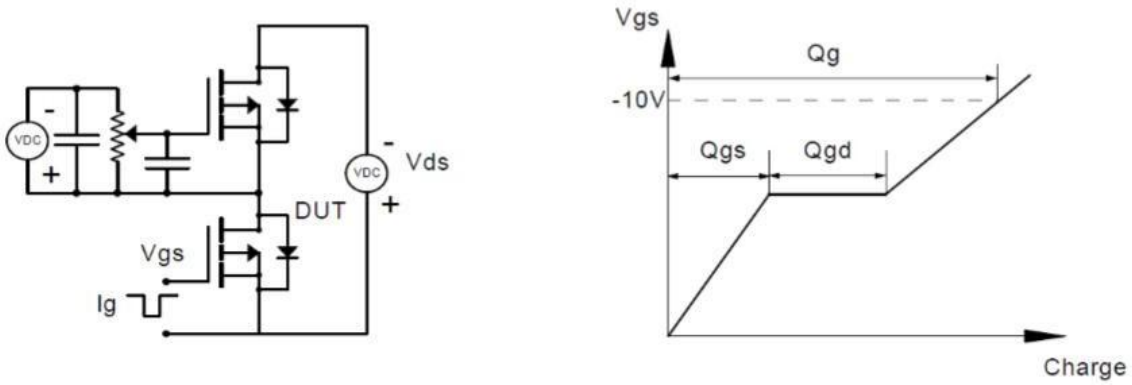


Figure 10. Maximum Safe Operating Area

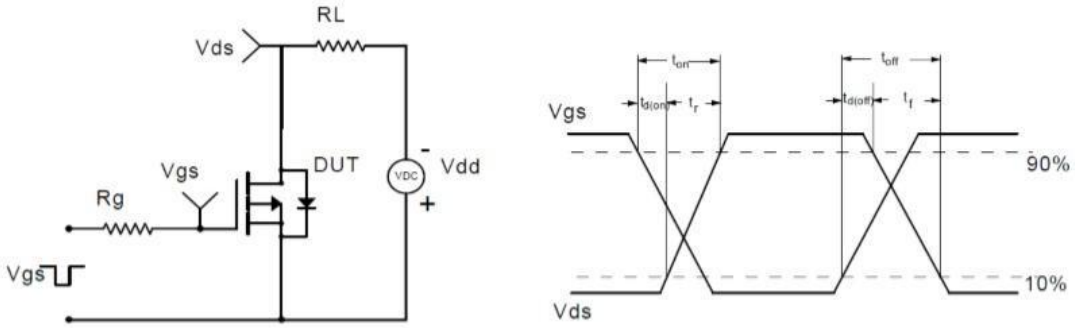


Test Circuit

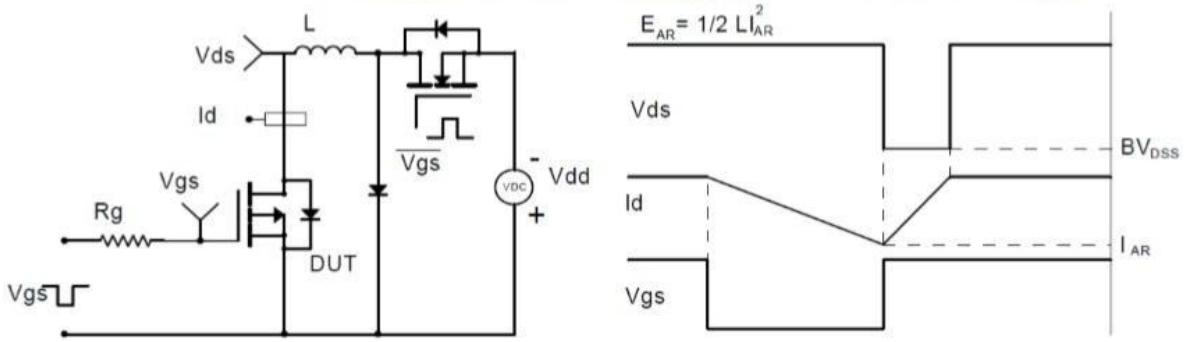
Gate Charge Test Circuit & Waveform



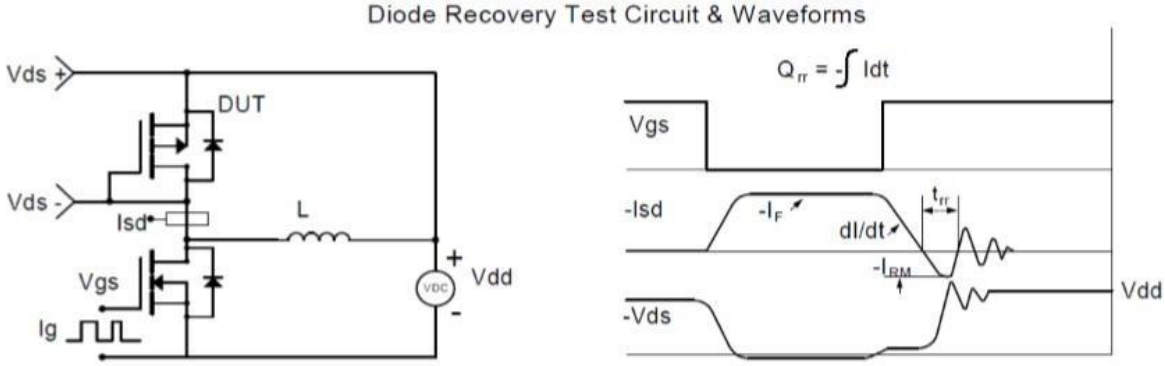
Resistive Switching Test Circuit & Waveforms



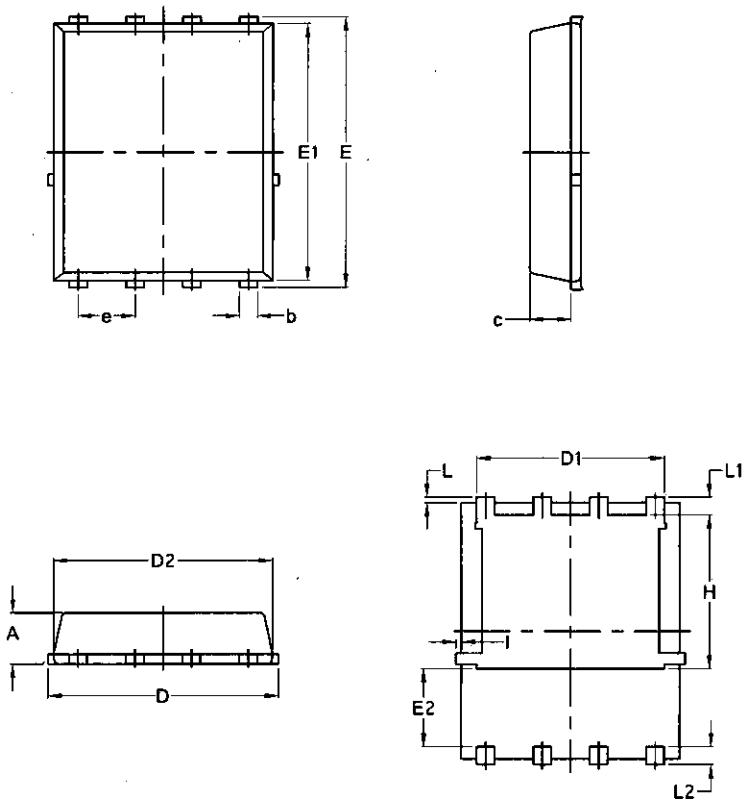
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Mechanical Data-PDFN5060-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070